REMARKS/ARGUMENTS

Claims 85 - 103 are pending in the application.

The rejection of claims 85-87, 89-93 and 99 under 35 U.S.C. 102(e) as being anticipated by Swamy (US 6,686,759) is respectfully traversed.

As made clear in the amendment filed June 24, 2005, the present invention is mainly for debugging or diagnosing two or more scan cores and the invention debugs or diagnoses "at-speed" delay faults, so each scan clock must comprise two system clock cycles, whereas to debug/diagnose stuck-type delay faults, each scan clock can comprise only one clock cycle. Thus, applicants' invention uses the term "selected fault type" that allows the DFD circuitry to generate required clock cycles -- "an ordered sequence of capture clocks."

Moreover, as further pointed out in the response filed June 24, 2005, with the advance in deep sub-micron manufacturing, an integrated circuit can now contain 30 to 50 clock domains (or scan cores) each controlled by one scan clock (or system clock). During debug or diagnosis, one can no longer assume that you can test <u>all</u> scan cores simultaneously, because the generated heat and test power could potentially damage the chip. Hence, applicants' claim 85 contains the limitations:

> ...a DFD selector for indicating <u>which said scan cores and said selected fault type</u> will be debugged or <u>diagnosed simultaneously</u>... (See claim 85, clause (a).)

In regard to the Swamy patent, in attempting to read the Swamy patent on applicants' claim, the Examiner contends that Swamy discloses:

> ...a DFD selector (multiplexer 62) having a plurality of inputs (TDO-1, TDO-2, TDO-3... connected to the internal circuit blocks (45-1, 45-2, 45-3...), and outputting a Test Data Output (TDO) signal 66 provided by IEEE Standard 1149.1 TAP 60, for debugging scan cores (46-1, 46-2, 46-3....) with their fault types.

This is not the case. Swamy's Fig. 2 discloses a circuit in which the inputs to the scan core's 46-1, 46-2, 46-3... are controlled by the demultiplexer 52 which outputs clock signals TCK-1, TCK-2, TCK-3... TCK-2_n to the cores selected by select register 56. The select register 56 also selects the corresponding outputs TDO-1, TDO-2, TDO-3...TDO-2_n inputs to the multiplexer 62 which are the test outputs from the scan cores 45-1, 45-2, 45-3, etc. Thus, the demultiplexer 52, select register 56 and multiplexer 62 assures that when a test clock TCK-1, for example, is applied to scan block circuit cores 45-1 that the output from that block TDO-1 is outputted from the multiplexer at the proper time. It has nothing to do with applicants' invention which involves a DFD selector indicating which sets of scan core and faults types will be debugged or diagnosed simultaneously. The Swamy reference says nothing about fault types. In fact, the term "fault" does not appear in the Swamy specification.

In essence, what the Examiner has done in attempting to read applicants' claim 85 on the Swamy reference is to pick out bits and

pieces, from the reference and assign functions to them for which there is no reasonable basis. Moreover, in seeking to read applicants' claim 85 on the Swamy reference, the Examiner has reversed the order of the Swamy parts and their function.

Whereas applicants' claim calls for a DFD selector for indicating which scan cores and selected fault types will be debugged or diagnosed simultaneously, note the Swamy reference is silent.

Whereas applicants' claim 85 calls for a multiplexer for connecting the DFD selector and the scan connector to a TAP (test access port) controller in the integrated circuit. Swamy uses his demultiplexer 52 and multiplexer 62 with an input register to select the demultiplexer clock output and assure that the multiplexer test data output are synchronized.

Applicants' claim 86 calls for a scan debug mode wherein the scan debug mode is set to a logic value 1 when the scan cores are to be diagnosed and set to a logic value 0 when the scan cores are not to be diagnosed. At column 7, line 60 *et seq*, Swamy states:

> The rest of the signals, Test Data Input 68, Test Mode Select 70, and Test Reset 72 are common to all the test access ports 60, and are preferably connected directly to their respective chip-level pins.

Nothing corresponding to the function recited in claim 86 is set out in this portion of the Swamy disclosure.

Claim 87 recites that the:

> ...TAP controller is constructed according to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out),

TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset)

which, as shown above, does not find a response in Swamy. Claim 89 depends from claim 87 and further restricts the DFD selector to shift register for two or more bits in each said scan core to indicate whether said scan core will be diagnosed and what said selected fault type shall be targeted which, as shown above, is not disclosed or suggested in the Swamy disclosure. Clearly, Swamy does not target any fault type in particular and does not seek to control which scan cores and which selected fault types will be debugged or diagnosed simultaneously.

Claims 90-92 depend from claim 87 and relate to the use of a plurality of multiplexers to stitch multiple scan chains together either as a serial scan chain or as multiple scan chains to share the same scan clock together. No such teaching or suggestion is shown in the Swamy reference. Claim 93 depends from claim 85 and specifies the scan connector further comprises selectively inserting an inverter and a lock-up element between any two multiple scan chains when stitched together to form a serial scan chain or a grouped scan chain wherein the lock-up element is selected from a D latch or D flip-flop. The terms "D latch" or "D flip-flop" do not even appear in the Swamy disclosure.

The rejection of claim 88 under 35 U.S.C. 103(a) as being unpatentable over Swamy is respectfully traversed. Again, Swamy does not even mention fault types and as explained above, applicants use the term "selected fault type" to allow the DFD

circuitry to generate the required ordered sequence of capture clock. No teaching or suggestion is found in the Swamy disclosure. While it may be true as the Examiner says that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate various fault conditions, it was not known in the art to indicate which scan cores and selected fault types "will be debugged or diagnosed simultaneously."

The rejection of claims 94-98 under 35 U.S.C. 103(a) as being unpatentable over Swamy in view of McLaurin et al (US 6,598,192) (hereinafter "McLaurin") is respectfully traversed. As shown extensively above, McLaurin neither discloses nor suggests a scan clock generator for generating an ordered sequence of capture clocks for connection to the scan clocks in the scan cores. Claim 94 characterizes the scan clock generator as comprising a clock phase generator and a scan clock controller. (See Fig. 7(a), sheet 1, and the ordered sequence of capture clock as shown in Figs. 7(b), 7(c), 7(d) and 7(e).) As stated in the paragraph bridging pages 23 and 24:

> ... As illustrated by pulses 733 to 735, this clocking scheme can reduce both peak power consumption and average power dissipation. During the capture cycle, clock-domain based signal-capture pulses 736 to 738 are applied at the frequency of TCK. This makes it possible to diagnose stuck-type faults, including stuck-at, bridging, or IDDQ faults.

No such teaching or suggestion is found in these references or any combination thereof.

The rejection of claims 100-103 under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,122,762) in view of Swamy is respectfully traversed.

Kim does not teach or suggest how to test "two or more" scan cores. As noted earlier, the present invention is mainly for simultaneously debugging or diagnosing two or more selected scan cores for selected fault types.

Claim 100 requires in step (c):

> ...issuing a first SHIFT command or a first plurality of SHIFT_CHAIN commands for shifting in a predetermined scan pattern to all scan cells within selected scan chains in said scan cores for diagnosis;

and in step (e):

> ...issuing a second SHIFT command or a second plurality of SHIFT_CHAIN commands for shifting a new predetermined scan pattern into and output response out of all said scan cells within said selected scan chains in said scan cores for diagnosis;

Neither Kim nor Swamy discloses or teaches how to provide such fault type detection in order for the debug operation.
It is required to provide a DFD selector to indicate which scan cores should be or should not be tested and for which actual fault should be detected simultaneously. This is reflected in claim 100 which recites:

> ...issuing a SELECT command for shifting in selected scan cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores;

It is not understood how the Examiner can read this language on Kim when the Examiner acknowledges that "Kim fails to disclose, 'two or

more scan cores each having a scan clock in an integrated circuit'." With integrated circuits containing 30 to 50 clock domains and it being impractical to test all scan cores simultaneously, applicants have shown how to test successfully selected scan cores and selected fault types simultaneously without exceeding power limitations.

This is not taught or suggested by Kim and not taught or suggested by Swamy for the reasons given earlier herein.

Claims 101-103 depend from claim 100 and are patentable for the same reasons.

In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,

Jim Zegeer

Jim Zegeer, Reg. No. 18,957
Attorney for Applicants

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

Date: July 17, 2006

In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.